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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,132	12/06/2001	Yuanlong Wang	MS-01CXT0161M	4787

53615 7590 12/14/2005

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,132	WANG ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9 and 11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-9 and 11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 9/21/05. Currently claims 5-9 and 11-18 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. *Claims 5-9 and 11-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Pekkala (US 2002/0172195).*

Regarding claim 5, Pekkala discloses plurality of point-to-point interface units comprising a computer module interface and a point-to-point interface; plurality of computer modules connected to the computer module interface of the plurality of point-to-point interface units; and bus emulator connected to the point-to-point interface of the plurality of point-to-point interface units (e.g., paragraph 55), the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108"), the at least one bus

emulator having a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase fan-out of the emulator, thereby increasing the signal length (e.g., para. 66, the bus bridge disclosed provides the ability claimed).

Regarding claim 6, Pekkala also discloses the point-to-point interface units comprise parallel-to-serial conversion units that detects the beginning of a data transfer cycle presented to the computer module interface (e.g., paragraph 8), and accepts a data field and an address field and a cycle-type indicator from the computer module interface (e.g., paragraph 166).

Regarding claim 7, Pekkala also discloses the plurality of point-to-point interface units comprise high-current parallel drivers (e.g., paragraph 10, "multiple IB channel adapters") capable of propagating data, address and data transfer cycle requests (e.g., paragraph 166).

Regarding claim 8, Pekkala also discloses the plurality of point-to-point interfaces interconnected by an internal bus (e.g., paragraph 9).

Regarding claim 9, Pekkala also discloses the arbiter for granting access to the internal bus to one of the plurality of point-to-point interfaces (e.g., paragraph 150).

Regarding claim 11, Pekkala discloses a point-to-point interface (e.g., paragraph 8) , the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108"), the at least one bus emulator having a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase fan-out of the emulator,

thereby increasing the signal length (e.g., para. 66, the bus bridge disclosed provides the ability claimed).

Regarding claim 12, Pekkala also discloses parallel-to-serial conversion unit that operates upon detecting the beginning of a data transfer cycle presented to the computer module interface (e.g., paragraph 8), and wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface (e.g., paragraph 166).

Regarding claim 13, Pekkala also discloses the point-to-point interface comprises high-current parallel drivers capable of propagating data, address and data transfer cycle requests (e.g., paragraph 10).

Regarding claim 14, Pekkala discloses a computer module interface and a point-to-point interface (e.g., paragraph 9) , the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108"), the at least one bus emulator having a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase fan-out of the emulator, thereby increasing the signal length (e.g., para. 66, the bus bridge disclosed provides the ability claimed).

Regarding claim 15, Pekkala also discloses parallel-to-serial conversion unit that operate upon detecting the beginning of a data transfer cycle presented to the computer module interface (e.g., paragraph 8), and wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer

module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface (e.g., paragraph 166).

Regarding claim 16, Pekkala also discloses the plurality of point-to-point interface units comprise high-current parallel drivers capable of propagating data, address and data transfer cycle requests (e.g., paragraph 10).

Regarding claim 17, Pekkala discloses an internal bus; and plurality of point-to-point interfaces interconnected by the internal bus (e.g., paragraph 8, "IBA"), , the emulator capable of supporting only one transfer at a time (e.g., paragraph 59, "coupled to one or more PCI buses on a host 102 rather than PCI buses 216 in an I/O unit 108"), a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase fan-out of the emulator, thereby increasing the signal length (e.g., para. 66, the bus bridge disclosed provides the ability claimed).

Regarding claim 18, Pekkala also discloses an arbiter for granting access to the internal bus to one of the plurality of point-to-point interfaces (e.g., paragraph 150).

Response to Arguments

Applicant's arguments filed 9/21/05 have been fully considered but they are not persuasive.

Regarding claim 5, Applicant argues that Pekkala does not disclose the amended feature of a cascade port; however, a new interpretation of Pekkala used above discloses this feature (e.g., para. 66, cited supra).

Regarding claims 11, 14, and 17, Applicant argues likewise for the amended feature; however, Examiner finds this feature in Pekkala (e.g., para. 66, cited supra).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

TIM VO
PRIMARY EXAMINER